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Solid-State Imaging Device ~~device~~

CROSS REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2002-280881, filed on September 26, 2002; the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

The present invention relates to a solid-state imaging device, and more particularly, it relates to a CMOS-sensor solid-state imaging device.

A CMOS sensor imaging device, for example, is provided with an image pickup unit (cell unit) that has pixels (unit cells) disposed in a two-dimensional array. The unit cells ~~has~~ have an opto-electric converter element which receives incident light and converts it into electric charges and a part which amplifies the electric charges to transmit them. The material ~~Material~~ for signal wirings (interconnections) to respectively activate the image pickup unit configured of the pixels in a 2D array are generally made of polysilicon (poly-Si) doped with ~~impurity~~ impurities.

However, a resistivity of the polysilicon ~~is considerably altered~~ changes considerably due to various factors such as an impurity doping condition, and is much higher than metal wirings in comparison, e.g., as high as $1.0 \times 10^{-3}\Omega$cm.

Thus, pixels ~~which are~~ located far ~~apart~~ from a

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driving circuit (or a driver circuit), which supplies ~~for developing~~ clock pulses to these pixels through the signal wirings, show significant voltage drop at the signal wirings as depicted in Fig. 10, and this prevents there being pulse voltage ~~from being obtained~~ sufficient to activate the pixels. More specifically, ~~as any of the pixels is farther from the driver circuit, the clock~~ the farther the pixels are from the driver circuit, the more reduced the amplitudes of the clock pulses transferred via the ~~signal wiring have their amplitudes reduced and waves transformed more, which~~ signal wiring, and the more transformed the waves. This in turn causes a problem of reduction of sensitivity in reading the electric charge in the pixels ~~apart~~ far from the driver circuit. This kind of drawback is defined as "shading".

To eliminate the drawback, as disclosed in Japanese Unexamined Patent Publication No. H02-5474, ~~devised is~~ there has been an improved arrangement of thicker polysilicon wiring for transmission of clock pulses from a driver circuit to pixels with reduced ~~resistance or another arrangement of~~ resistance. In another arrangement, dual driver circuits are located on opposite flanks of an image pickup unit to develop clock pulses to pixels.

However, ~~the polysilicon wiring,~~ when increased in thickness, ~~adds up as much an area as required for an occupation by the wiring~~ the polysilicon wiring takes up a larger area, which is disadvantageous in miniaturizing the resultant device. Additionally, the arrangement of the dual driver circuits on the opposite sides of the

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image pickup unit ~~has to keep an enlarged area as much as two of the driver~~ requires occupying an area large enough for two driver circuits, and this also prevents a miniaturization of the chip.

SUMMARY OF THE INVENTION

According to an embodiment of the present invention, there is provided a solid-state imaging device, comprising:

an image pickup unit having unit cells including opto-electrical converter elements, said unit cells being disposed in a two-dimensional array,

a selection line made of polysilicon for selectively determining the unit cells in the same row within the image pickup unit,

a read-out line made of polysilicon for reading out an electric charge accumulated in the opto-electrical converter elements of the unit cells in the same row within the image pickup unit,

a signal line transmitting pixel signals produced from the unit cells in the same row within the image pickup unit,

a reset line made of polysilicon for discharging the unit cells in the same row within the image pickup unit down to ~~the~~ a desired voltage level,

a driver circuit located on one side of the image pickup unit for supplying drive signals to the read-out line, the selection line, and the reset line, respectively, and

a read-out auxiliary wiring disposed along at least

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the read-out line and electrically connected to the read-out line at a plurality of junctions, the read-out auxiliary wiring being of ~~relatively~~ comparatively lower electric resistivity than the read-out line.

According to another embodiment of the present invention, there is provided a solid-state imaging device, comprising:

an image pickup unit having unit cells including first and second opto-electrical converter elements, said unit cells being disposed in a two-dimensional array,

a selection line made of polysilicon for selectively determining the unit cells in the same row within the image pickup unit,

first and second read-out lines made of polysilicon for reading out an electric charge accumulated in the first and second opto-electrical converter elements of the unit cells in the same row within the image pickup unit,

a signal line transmitting pixel signals produced from the unit cells in the same row within the image pickup unit,

a reset line made of polysilicon for discharging the unit cells in the same row within the image pickup unit down to ~~the~~ a desired voltage level,

a driver circuit located on one side of the image pickup unit for supplying drive signals to the first and second read-out lines, the selection line, and the reset line, respectively,

first and second read-out auxiliary wirings

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disposed along at least the first and second read-out lines, respectively, and electrically connected to the first and second read-out lines, respectively, the first and second read-out auxiliary wirings being of ~~relatively~~ comparatively lower electric resistivity than the first and second read-out lines, respectively.

According to a further embodiment of the present invention, there is provided a solid-state imaging device, comprising:

an image pickup unit having unit cells including opto-electrical converter elements, and a sensing unit to detect charges accumulated in the ~~opt-electrical~~ opto-electrical converter elements, said unit cells being disposed in a two-dimensional array,

a selection line made of polysilicon for selectively determining the unit cells in the same row within the image pickup unit,

a read-out line made of polysilicon for reading out an electric charge accumulated in the opto-electrical converter elements of the unit cells in the same row within the image pickup unit,

a signal line transmitting pixel signals produced from the unit cells in the same row within the image pickup unit,

a reset line made of polysilicon for discharging the unit cells in the same row within the image pickup unit down to ~~the~~ a desired voltage level,

a driver circuit located on one side of the image pickup unit for supplying drive signals to the read-out line, the selection line, and the reset line,

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respectively, and

a read-out auxiliary wiring disposed along at least the read-out line and electrically connected to the read-out line at a plurality of junctions, the read-out auxiliary wiring being of ~~relatively~~ comparatively lower electric resistivity than the read-out line;

said reset line and said read-out line being symmetrical about a sensing unit interpolated at their respective extensions of centers, and said read-out line and said selection line being symmetrical about the opto-electrical converter elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram showing an equivalent circuit of a CMOS sensor provided as a first embodiment according to the present invention;

Fig. 2 is a plan view illustrating an exemplary configuration of a major portion of the CMOS sensor of Fig. 1;

Fig. 3 is a vertical ~~cross-sectional~~ cross-sectional view taken along the line A1-A2 and B1-B2 of Fig. 2;

Fig. 4 is a graph showing a relation of a distance from a driver circuit to a level of voltage supply in a cell unit of the CMOS sensor;

Fig. 5 is a diagram showing an equivalent circuit of a single pixel in the CMOS sensor provided as a second embodiment according to the present invention;

Fig. 6 is a plan view showing an exemplary configuration of a major portion of the single pixel of

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Fig. 5;

Fig. 7 is a vertical sectional view taken along the line C1-C2 of Fig. 6;

Fig. 8 is a diagram of an equivalent circuit showing a single exemplary pixel in the CMOS sensor provided as a third embodiment according to the present invention;

Fig. 9 is a plan view showing an exemplary configuration of a major portion of a single pixel of Fig. 8; and

Fig. 10 is a graph illustrating a relation of a distance from a driver circuit to a level of voltage supply in a cell unit of the prior art CMOS sensor.

DETAILED DESCRIPTION

Referring to the accompanying drawings, embodiments of the present invention will now be described in detail.

Fig. 1 is an equivalent circuit diagram showing an embodiment (first embodiment) of a CMOS sensor to which the present invention is applied.

As depicted in Fig. 1, a CMOS sensor 1 reads out electric charges accumulated in each of photodiodes (opto-electric converting elements) 8 by a driver circuit and transmits the electric charges via vertical and horizontal signal lines to sequentially output them ~~to external~~ externally.

First, a configuration of the CMOS sensor 1 will be explained.

The CMOS sensor 1 has a cell unit (image pickup unit) 3 that has a plurality of unit cells (pixels) 2

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disposed in a two-dimensional array, the unit cells 2 having photodiodes 8. As can be seen, the pixels denoted by reference symbols 2a and 2b are those centered in the cell unit 3. The pixels 2 include ~~the~~ a desired number (e.g., one) of the photodiodes 8 capable of accumulating received light from the outside and opto-electrically converting it into signals of ~~the electric charge to~~ an electric charge and accumulate them. Also, the pixels 2, as depicted in Fig. 1, have their respective signal detection circuitries each consisting of ~~the~~ a desired number (e.g., four) of transistors 9, 10, 11 and 12. Thus, in this case, each of the signal detection circuitries has a ~~the~~ reset transistor 9 used to discharge ~~from~~ the pixel 2 to reduce the unnecessary charges, the read-out transistor to read out the electric charge accumulated in the photodiode 8, ~~the~~ an amplification transistor 11 amplifying the readout electric charge from ~~the~~ a read-out transistor 10 to produce pixel signals via vertical signal lines 6, and ~~the~~ a vertical selection transistor 12 selectively determining which one(s) of the pixels should be accessed to read out the pixel signals.

A structure of the signal detection circuitry will be detailed below.

~~The read-out transistor 10 has its one end~~ One end of the read-out transistor 10 is connected to a cathode of the photodiode 8 and the other end is connected to a sensing node (sensing unit) 7 which is an n^+ region, to detect the electric charge accumulated in the photodiode 8. An anode of the photodiode 8 is grounded. The

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sensing node 7 is connected to a gate electrode of the amplification transistor 11 to feed the detected electric charge from the sensing node 7 to the gate electrode of the amplification transistor 11. ~~The reset transistor 9 has its one end~~ One end of the reset transistor 9 is connected to the sensing node 7 and the other end is connected to a predetermined reference potential. Configured in this manner, the reset transistor 9 allows the sensing node 7 and the photodiode 8 to discharge unnecessary charges ~~remained~~ remaining in the sensing node 7 and in the photodiode 8.

The vertical selection transistor 12 has its one end connected to the reference potential and the other end connected to one end (first end) of the amplification transistor 11. When turning on, the vertical selection transistor 12 feeds the reference potential to ~~that end of~~ the end connected to the amplification transistor 11.

Within the cell unit 3, where pixels 2 each configured in the aforementioned manner have been disposed in a two-dimensional manner, there is provided a reset line 13 to which the reset transistors 9 in the same row have their respective gate electrodes connected in common. Also provided are a read-out line 14 to which the read-out transistors 10 in the same row have their respective gate electrodes connected in common, and a selection line (address line) 15 to which the vertical selection transistors 12 in the same row have their respective gate electrodes connected in common. The reset line 13, the read-out line 14, and the selection

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line 15 are all made of polysilicon doped with an impurity. In the cell unit 3, also, a plurality of vertical lines 6 are placed in parallel, one for each row of the pixels connected thereto in common, so as to transfer the pixel signals ~~taken out~~ received from the photodiodes 8 in the pixels 2 and then amplified, to a horizontal signal line 18 in a lower portion of the cell unit 3, as illustrated in the figure.

In a left portion of the cell unit 3 as shown in the figure, a clock driver 5 is provided to feed clock pulses to the read-out line 14 and the selection line 15, respectively. The clock driver 5 is provided with a vertical resister 4a that functions to sequentially select the pixels 2 of the same row at a time. Specifically, the vertical resister 4a designates a row so as to activate the clock driver for the designated row, thereby supplying clock pulses to the associated activation lines. In parallel with a full extension of the read-out line 14 of high resistivity, aluminum auxiliary wiring 19 of relatively low resistivity is provided, which is electrically connected to the read-out line 14 at the outside of and at lateral sides of the cell unit 3. In this way, with the aluminum wiring of low resistivity being juxtaposed with the read-out line 14 of high resistivity and electrically connected with the same at their respective opposite ends, the read-out line 14 provides almost the same potential at the lateral ends of the cell unit 3, which permits supply of clock pulses of sufficient voltage and satisfactory waveform to all the transistors 10

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connected to the read-out line 14.

In the lower part of the cell unit 3, the horizontal signal line 18 is provided to externally transfer the pixel signals that are read out from the pixels 2 in the same column to the vertical signal lines 6. The vertical signal lines 6 are connected to the horizontal signal line 18 by intervening horizontal selection transistors 16, and the horizontal selection transistors 16 have their respective gate electrodes connected to a horizontal register 4b that functions to selectively determine the horizontal selection transistors 16 in a sequence depending upon given clock pulses.

Now, an operation of the aforementioned device will be described.

First, the pixels 2 in the same selected row have their photodiodes 8 and sensing node 7 discharged down to ~~the~~ a desired level. More specifically, the read-out transistors 10 and reset transistors 9 in the same selected row receive clock pulses produced from the clock driver 5 for a certain period of time to turn on this set of the read-out and reset transistors 10 and 9. This causes the photodiodes 8 to discharge the unnecessary charges via the read-out and reset transistors 10 and 9 and also causes the sensing node 7 to discharge the unnecessary charges via the reset transistors 9 to the reference potential coupled to the reset transistors 9.

Then, the photodiodes 8 are effected to receive light and opto-electrically convert the incident light

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into signals of the electric ~~charge~~ charges that are to be accumulated.

After that, the clock pulses from the clock driver 5 are applied to the selection lines 15 in the same selected row to turn on the vertical selection transistors 12 connected to the selection lines 15, respectively. Once the vertical selection transistors 12 are turned on, the reference potential at one end of each vertical selection transistor 12 is fed to the first end of the amplification transistor 11 connected to the other end of the transistor 12.

In addition, the accumulated electric charge in the photodiodes 8 of the pixels 2 in the same selected row are read out. More specifically, the clock pulses from the clock driver 5 are supplied to the read-out lines 14 in the same selected row for a certain period of time to turn on the read-out transistors 10 connected to the read-out lines 14, respectively. Once the read-out transistors 10 are turned on, the accumulated electric charge in the photodiode 8 connected to one end of each read-out transistor 10 is taken out via the transistor 10. As mentioned above, the read-out ~~line~~ lines 14, which are connected to and shared by the read-out transistors 10, ~~exhibits~~ exhibit no voltage drop at ~~its~~ their opposite ends by virtue of the aluminum auxiliary wiring 19 and ~~retains~~ retain almost the same potential at both ~~the~~ ends, and hence, the read-out transistors 10 receive the clock pulses of sufficient voltage and satisfactory waveform to read out the accumulated electric charge in the photodiodes 8. As a consequence,

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the accumulated electric charge in each of the photodiodes 8 can be assuredly read out by each of the read-out transistors 10.

The readout result by the transistor 10 of the accumulated electric charge in the photodiode 8 is transferred to a gate of each of the amplification transistors 11 in the same selected row. In this way, a gate potential at the amplification transistor 11 is varied, and voltage signals based upon potential variations (i.e., pixel signals) are ~~produced~~ transmitted to the vertical signal line 6 connected to the other end (second end) of the amplification transistor 11.

The pixel signals ~~produced~~ transmitted from the amplification transistor 11 to the associated vertical signal line 6 are sequentially transferred to the horizontal signal line 18 via the associated horizontal selection transistor 16 connected to one end of the vertical signal line 6. Thus, the clock pulses from the horizontal register 4b connected to the plurality of the horizontal selection transistors 16 selectively determine a sequence of the transistors 16 to which the pixel signals from the vertical signal lines 6 are sequentially fed to the horizontal signal line 18. The pixel signals sent from the vertical signal lines 6 to the horizontal signal line 18 are transferred to an intermediate component such as an amplification circuit not shown but connected to an export end of the horizontal signal line 18, and are eventually ~~taken~~ output externally.

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Fig. 2 is a plan view showing an exemplary configuration of a major portion 20 with the aluminum auxiliary wiring of Fig. 1. Fig. 3A is a vertical ~~cross sectional~~ cross-sectional view taken along the line B1-B2 of Fig. 2 while Fig. 3B is a vertical ~~cross sectional~~ cross-sectional view taken along the line A1-A2.

As shown in Fig. 2, the read-out line 14 and the juxtaposed aluminum auxiliary wiring 19 along the full ~~extension~~ length of the same are electrically connected to each other, with contacts 21(1) and 21(2) being interposed at external lateral sides of the cell unit 3. This is specified in Fig. 3B showing a vertical ~~cross section~~ cross-sectional along the line A1-A2 of Fig. 2 where the aluminum auxiliary wiring 19 along the full length of the read-out line 14 has its one end electrically coupled to the same by a tungsten plug 25 that is embedded in silicon oxide film 23 serving as an interlayer insulation film. Also, the aluminum auxiliary wiring 19 has the other end electrically connected to the read-out line 14 in the similar manner. The aluminum auxiliary wiring is located at some interval above the read-out line 14 so as not to ~~give~~ have adverse effects upon received light on the photodiodes 8, as depicted in Fig. 3A in a vertical ~~cross section~~ cross-sectional along the line B1-B2 of Fig. 2. A configuration of the read-out transistor 10 in Fig. 3A will be outlined below.

The read-out line 14 is embedded in the silicon oxide film 23 above a region between the photodiode 8 and the sensing node 7 formed in the p substrate 22. The read-out line 14 also serves as gate electrodes of the

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read-out transistors 10. As stated above, the aluminum auxiliary wiring 19 is placed above the read-out line 14, with the intervening silicon oxide film 23, and ~~besides~~ in addition, silicon oxide film 24 overlies and covers the aluminum auxiliary wiring 19.

In this structure where the read-out line 14 and the aluminum auxiliary wiring 19 are juxtaposed along their respective full ~~extensions~~ lengths, a position where voltage of the clock pulses fed by the read-out line 14 drops the most is the center of the cell unit 3, as shown in Fig. 4. This will be described below in more detail.

A resistivity of aluminum line extending along the read-out line 14 is relatively low, e.g., as low as $2.655 \times 10^{-6}\Omega$cm, and almost no voltage drop is observed throughout its full length. Thus, the read-out line 14 exhibits almost the same potential at its ~~the~~ opposite ends in contact with the aluminum auxiliary wiring 19 and at the external lateral sides of the cell unit 3. Hence, voltage of the clock pulses transferred by the read-out line 14 drops the most in the mid point equidistant from the contacts 21(1) and 21(2) of the aluminum auxiliary wiring 19 with the read-out line 14 (see Fig. 2). This means that the pixels 2a and 2b centered in the cell unit 3 (see Fig. 1) are those that are supplied with ~~voltage the least~~ the least voltage. The least voltage applied to the pixels 2a and 2b, as will be recognized in Figs. 10 and 4, drops by approximately ~~a~~ half, compared with that applied to pixels in the prior art CMOS sensor, and is sufficient

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to read out the electric charge.

As has been described, in an aspect of the first embodiment according to the present invention, since the read-out line 14 of high resistivity and the aluminum auxiliary wiring of low resistivity are juxtaposed along each other and electrically connected to each other at the external lateral sides of the cell unit 3, the device ensures ~~to attain a feature almost the same as that is attainable~~ almost the same features as are attainable in a device where the driver circuit ~~are~~ is disposed on either of the lateral sides of the cell unit 3. Thus, the CMOS sensor of this invention can develop clock pulses retaining sufficient amplitude and square waveform even in the center of its cell unit, which ~~that~~ usually encounters the largest degradation of the clock waveform. Resultantly, during the accelerated operation, signal transmission can be maintained appropriately. In addition to that, the aluminum auxiliary wiring is positioned right above the read-out line 14; that is, it is located in a position that does not affect ~~without affecting~~ light receiving efficiency in the photodiodes 8, and therefore, the light receiving efficiency in the photodiodes 8 would not be reduced significantly.

Although, in the aforementioned first embodiment, the aluminum auxiliary wiring 19 is provided in a position relative to the read-out line 14, it may similarly be in relation with the reset line 13 or the selection line 15. Especially, the reset transistor 9 connected to the reset line 13 requires relatively higher voltage as much as 2.8 V, for example, than the

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read-out transistor 10 of which drive voltage is 1 to 1.2 V. Thus, by electrically connecting the aluminum auxiliary wiring to the reset line 13 ~~of which required drive voltage is greater~~ which requires a greater drive voltage, the resultant CMOS sensor can attain improved signal property effectively.

Fig. 5 is an equivalent circuit diagram showing an exemplary pixel in another type of the CMOS sensor to which the present invention is applied ~~to make it (or a second embodiment) distinguishable~~ (or a second embodiment), making it distinguishable from the first embodiment. This CMOS sensor is ~~that~~ one which has two ~~of~~ photodiodes and two ~~of~~ read-out transistors in each of the pixels. In this embodiment, an effective application of the present invention to such a CMOS sensor is intended to avoid adverse effect due to an incident angle of light upon the photodiodes in the pixel as much as possible.

Fig. 6 is a plan view showing an exemplary structure of a major portion 20 of the pixel in Fig. 5 while Fig. 7 is a vertical ~~cross sectional~~ cross-sectional view taken along the line C1-C2 of Fig. 6.

A configuration of pixels 2 of the CMOS sensor will be outlined below.

As depicted in Fig. 5, each of the pixels 2 has two photodiodes 8(1) and 8(2) serving as light receiving elements. Two read-out transistors 10(1) and 10(2) are provided to read electric charges accumulated in the two photodiodes 8(1) and 8(2). Two read-out lines 14 (1) and 14(2) are provided to activate the read-out transistors

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10(1) and 10(2), respectively, which are commonly connected to a sensing node 7. Configured in this manner, the electric charges read out from the photodiodes 8(1) and 8(2), respectively, are synthesized in the sensing node 7 and fed as signals of electric charge to a gate of an amplification transistor 11 connected to the sensing node 7. Aluminum auxiliary wirings 19(1) to 19(4) are juxtaposed and electrically connected at lateral sides of the cell unit 3 with driving wirings that drive the pixels 2, namely, the read-out lines 14(1) and 14(2), the reset line 13, and the selection line 15. The remaining components are similar in structure and operation to their respective counterparts depicted in Fig. 1, and descriptions of them are omitted.

The driving wirings, or the readout lines 14(1) and 14(2), and the reset line 13, and the selection line 15 ~~are deployed in practice~~ are practically arranged as follows.

As shown in Fig. 6, the reset line 13 and the read-out line 14(1) are located symmetrically about the photodiode 8(1), and similarly, the read-out line 14(2) and the selection line 15 are about the photodiode 8(2). Thus, the aluminum auxiliary wirings 19(1) to 19(4) are respectively provided in a symmetrical deployment relative to the arrangement of the associated driving wirings. Also, as shown in Fig. 7, a group of the read-out lines 14(1) and 14(2), the reset line 13, and the selection line 15, and another group of the aluminum auxiliary wirings 19(1) to 19(4) are in the same hierarchy level, respectively. Configured in this manner

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where, about the photodiodes 8(1) and 8(2) and their respective vertical extensions, structures on opposite sides are symmetrical, the adverse effect upon light receiving efficiency due to an incident angle of light on the photodiodes 8(1) and 8(2) can be avoided.

Specifically, as shown in Fig. 7, when light beam 30 directed from a certain direction is incident upon the photodiodes 8(1) and 8(2), ~~respectively,~~ the aluminum auxiliary wirings 19(1) and 19(4) along the optical path reflect (or shield) part of the light beam 30. Also, when directed from a direction almost symmetrically opposite to the beam 30 about a vertical center axis of each photodiode, another light beam 31 incident upon the photodiodes 8(1) and 8(2) is partly shielded like the light beam 30. Thus, the light receiving efficiency is almost even on lateral sides of the photodiodes 8(1) and 8(2) without adverse effect ~~on~~ related to the incident angle of received light.

Without this structural symmetry about the photodiodes 8(1) and 8(2), the deposited interlayer insulation films 23 and 24 lack uniformity in thickness, being varied from a region overlying the wirings to a region without them, which would give adverse effects due to the incident angle of light. This would cause unevenness in sensitivity ~~to~~ and lead to a degradation of optical properties and an eventual production of a poor quality image. ~~In~~ From this point of view, the lateral structural symmetry about the photodiodes is effective in suppressing possible propagation of adverse ~~effect~~ effects due to the incident angle of light and

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avoiding a degradation of optical properties.

~~Fig~~ Fig. 8 is an equivalent circuit diagram showing an exemplary pixel in another type of the CMOS sensor to which the present invention is applied to make it (or a third embodiment) distinguishable from the first embodiment. This CMOS sensor ~~is that which~~ has a single photodiode and a single read-out transistor in each of the pixels.

Fig. 9 is a plan view showing an exemplary structure of a major portion 20 of one of the pixels.

As shown in Fig. 8, each of pixels 2 in the CMOS sensor has a single photodiode 8 serving as a light receiving element and also has a single read-out transistor 10 to read out electric charge accumulated in the photodiode 8. A read-out line 14 is provided to activate the read-out transistor 10 which is connected to a sensing node 7.

Configured in this manner, electric charge read out from the photodiode 8 is synthesized in the sensing node 7 and then fed as signals of electric charge to a gate of an amplification transistor 11 that is connected to the sensing node 7. Aluminum auxiliary wirings 19(1) to 19(4) are juxtaposed and electrically connected at lateral sides of the cell unit 3 with driving wirings that drive the pixels 2, namely, the read-out lines 14, the reset line 13, and the selection line 15. The remaining components are similar in structure and operation to their respective counterparts depicted in Fig. 1, and detailed descriptions of them will be omitted.

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A practical deployment of the driving wirings, or the readout line 14, and the reset line 13, and the selection line 15 will be described with reference to Fig. 9 as follows.

As shown in Fig. 9, the reset line 13 and the read-out line 14 are symmetrical about the sensing unit interpolated at their respective extensions of centers, and the read-out line 14 and the selection line 15 are also symmetrical about the photodiode 8. The aluminum auxiliary wirings 19(1) to 19(4) are similarly provided symmetrically in relation to a deployment of their respective associated driving wirings.

An operation in such an arrangement of this embodiment is similar to that described in conjunction with Fig. 7, and therefore, an additional description will be omitted.

In an aspect of the third embodiment according to the present invention where the driving wirings and the aluminum auxiliary wirings are provided in a lateral symmetrical deployment about the photodiode, a CMOS sensor of enhanced uniformity in sensitivity can be provided to enable appropriate transmission of signals of reduced deterioration of clock waveform.

As has been recognized from the above statement, in accordance with embodiments of the present invention, the following features are attained.

Configured as having driver circuitries (i.e., a vertical register and a clock driver) simply on a single side of a cell unit (i.e., an image pickup unit), the device ensures that produced clock pulses keep stable

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~~amplitude as in~~ amplitude, similar to an arrangement with the driver circuitries on opposite sides of the cell unit. Thus, without a further enlargement of chip area, the device permits the produced pulses to be sent to pixels disposed laterally opposite to the driver circuitries while avoiding possibly propagating voltage drop throughout their transmission passages.

The embodiments of the invention eliminate complicated treatments such as providing shunt wiring within a cell unit and accordingly takes away any further burden of necessarily ~~forming a numeral number of contacts, thereby retaining the yield of the process~~ forming numerous contacts, thereby retaining yield in the process.

Also, configured as having driver circuitries on one side of the image pickup unit where unit cells with opto-electrical converter elements are disposed in a two-dimensional array, the device is provided with auxiliary wirings of low resistance that are juxtaposed and electrically connected with associated driving wirings serving respectively to drive the unit cells in the same row ~~at a time~~ all at once, and hence, the device permits produced clock pulses to be sent to the unit cells connected to the driving wirings without possible propagation of a deterioration of clock waveform. Thus, without a further enlargement of chip area, the device of enhanced performance during accelerated operation can be provided.